

WHAT IS CLAIMED IS:

1 1. A processing core that executes a compare instruction, the
2 processing core comprising:
3 a plurality of general-purpose registers comprising a first input operand
4 register, a second input operand register and an output operand register;
5 a register file comprising the plurality of general-purpose registers;
6 comparison logic coupled to the register file, wherein the comparison logic
7 tests for at least two of the following relationships: less than, equal to, greater than and no
8 valid relationship;
9 decode logic which selects the output operand register from the plurality of
10 general-purpose registers; and
11 a store path between the comparison logic and the selected output operand
12 register.

1 2. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein a very long instruction word includes a plurality of compare
3 instructions.

1 3. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein decode logic selects the first and second input operand registers
3 from the plurality of general-purpose registers.

1 4. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein the processing core issues a plurality of compare instructions at
3 one time.

1 5. The processing core that executes the compare instruction as set
2 forth in claim 1, further comprising:
3 a first load path between the first input operand register and comparison
4 logic; and
5 a second load path between the second input operand register and
6 comparison logic.

1 6. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein the output operator register stores a value indicating a

3 relationship between the first and second input operator registers which is at least one of
4 greater than, less than, equal to and not a number.

1 7. The processing core that executes the compare instruction as set
2 forth in claim 6, wherein the not a number value indicates a comparison between the first
3 and second input operands that cannot be made.

1 8. The processing core that executes the compare instruction as set
2 forth in claim 6, wherein the value is an integer.

1 9. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein:
3 the first input operand register is a double precision floating point data
4 type;
5 the second input operand register is a single precision floating point data
6 type; and
7 the output operand register is a double precision floating point data type.

1 10. The processing core that executes the compare instruction as set
2 forth in claim 1, further comprising a plurality of processing paths that are coupled to the
3 register file.

1 11. The processing core that executes the compare instruction as set
2 forth in claim 1, wherein the register file comprises special purpose registers which
3 cannot store an output operand.

1 12. A method for performing a compare operation, the method
2 comprising steps of:
3 decoding a compare instruction;
4 configuring first and second paths between a register file and comparison
5 logic;
6 configuring a third path between the comparison logic and the register file;
7 comparing a first input operand and a second input operand to produce a
8 result which indicates an absence of at least three mathematical relationships between the
9 first input operand and the second input operand; and

10 coupling an output operand to a general-purpose register in the register
11 file.

1 13. The method for performing the compare operation as set forth in
2 claim 12, the method further comprising a step of enabling the comparison logic in an
3 arithmetic logic unit.

1 14. The method for performing the compare operation as set forth in
2 claim 12, wherein the configuring steps each comprise a step of addressing a general-
3 purpose register in the register file.

1 15. The method for performing the compare operation as set forth in
2 claim 12, wherein a very long instruction word comprises the compare operation.

1 16. The method for performing the compare operation as set forth in
2 claim 12, wherein the comparing step comprises a step of converting a data type of at
3 least one of the first and second input operands.

1 17. A method for executing a compare instruction in a processor, the
2 method comprising steps of:
3 issuing the compare instruction;
4 comparing a first input operand and a second input operand to determine at
5 least two mathematical relationships between the first and second input operands;
6 determining an output operand indicative of the mathematical
7 relationships; and
8 storing the output operand in a general-purpose register of a register file.

1 18. The method for executing the compare instruction in the processor
2 as set forth in claim 17, wherein the comparing step comprises:
3 determining if the first input operand is less than the second input operand;
4 determining if the first input operand is greater than the second input
5 operand;
6 determining if the first input operand is equal to the second input operand;
7 and
8 determining if there is no valid relationship between the first input operand
9 and the second input operand.

1 19. The method for executing the compare instruction in the processor
2 as set forth in claim 17, wherein the compare instruction is a very long instruction word
3 which comprises a plurality of compare instructions which are processed in parallel down
4 separate processing paths.

1 20. The method for executing the compare instruction in the processor
2 as set forth in claim 17, wherein the general-purpose register is used to store operators
3 from other types of instructions.